

Virtual 4 Gb/s Ethernet MAC

This application note outlines how to use the ChipEnet SM1000 Gigabit Ethernet MAC to create a virtual 4 Gb/s Ethernet MAC.

Introduction

As of this writing, 5-2006, 10 Gb/s Ethernet is in its infancy. Components are expensive and usage in FPGA difficult. The easy and cost effective solution to higher bandwidth Ethernet is to group four 1 Gb/s MACs together to form a virtual 4 Gb/s Ethernet MAC. Using four ChipEnet SM1000 MACs requires less than 25,000 gates and 48 to 80 signal pins. The data interface is a convenient 32 bit format and only 4 Cat 5 cables are needed. This relatively low increase in gate and pin count is rewarded by a significant 4 Gb/s bandwidth. Not quite as good as 10 Gb/s in bandwidth but a much better value proposition suitable for implementation right now. The PHYs and RJ45 connectors are available at low cost and signal integrity is not an issue. No TCP/IP processing is needed and no driver programming is required.

Block Diagram of Virtual 4 Gb/s Ethernet MAC

Figure 1 show the overall block diagram of the virtual 4 Gb/s Ethernet MAC. Four instances of the ChipEnet SM1000 Ethernet MACs are instantiated in one FPGA. Each MAC contains a 128 byte or 2K byte read fifo, depending on the MAC, and a 128 byte or 2K byte write fifo. The fifos are all clocked by the same clock. A 32 bit word to be written into the virtual 4 Gb/s MAC is distributed between the four 1 Gb/s MACs. Byte 0 goes to the first MAC and byte 3 goes to the last MAC. The write fifo signal is connected to all four MACs so all four write fifos are always written in sync. The receive fifo empty flag of all four MACs are ORed together to form the receive fifo empty flag for the virtual 4 Gb/s MAC. Anytime one of the MAC has an empty receive fifo, the empty flag will be asserted. Only when all four MACs have valid data will the empty flag be low. All four MACs also share identical 125 MHz TX clock which is used to send data to the PHYs. The interface between the MAC and the PHY is 20 pins if MII interface is used and 12 pins if RMII

interface is used. However, RMI is not standardized so only certain PHY may be used, e.g. National DP 83865. The four Cat 5 cables should be of equal length and from the same roll of cables if possible. This will insure minimum cable skew.

The virtual 4 Gb/s Ethernet MAC may be used to connect two FPGA systems together or connect a FPGA system to a server. The server obviously need to have four Gb/s Ethernet ports. The server software will simply open four sockets, bind each socket to one of the Gb/s Ethernet ports and distribute the bytes of data between the four sockets. 4 Gb/s of bandwidth is quite a bit and may overwhelm a server that is not fast enough to handle it. A switch with at least eight Gb/s ports may also be used to make connections.

For additional details, take a look at www.chipEnet.com .

Conclusion

Grouping together four ChipEnet SM1000 Gb/s Ethernet MACs offer an easy and low cost method of achieving 4 Gb/s Ethernet bandwidth. Gate count and pin count are low and the data interface is a convenient 32 bits in width. Connection through an optional Ethernet switch may be made to another FPGA or to a server running simple socket based software. No TCP/IP processing is needed and no driver programming is required.

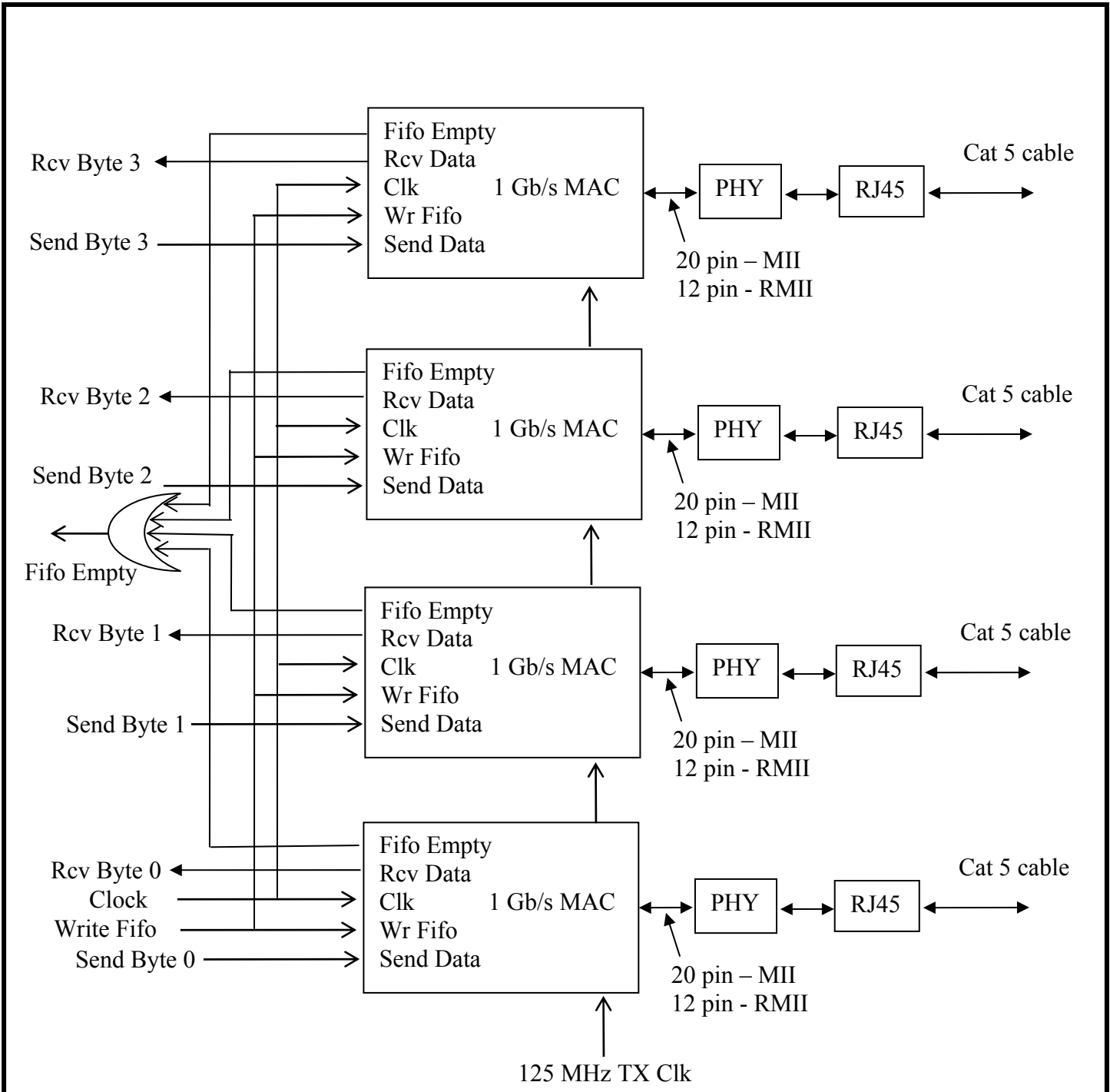


Figure 1. 4 Gb/s Virtual Ethernet MAC